IN THE CLAIMS

1. (withdrawn) A varactor comprising:

a silicon layer;

a P- well in the silicon layer;

first and second N+ regions in the silicon layer, wherein the first N+ region forms a first N+/P- junction with the P- well, and wherein the second N+ region forms a second N+/P- junction with the P- well;

a gate oxide above the P- well; and,

a silicon gate above the gate oxide.

2. (withdrawn) The varactor of claim 1 wherein the silicon gate comprises a polysilicon gate.

3. (withdrawn) The varactor of claim 1 wherein the silicon layer is formed over an insulation layer so that the silicon layer and the insulation layer together form an SOI structure.

4. (withdrawn) The varactor of claim 3 wherein the insulation layer is formed over a layer of high resistivity silicon.

5. (withdrawn) The varactor of claim 1 wherein the silicon layer is formed from bulk silicon.

6. (withdrawn) The varactor of claim 1 wherein the silicon layer is formed over a sapphire layer so that the silicon layer and the sapphire layer together form an SOS structure.

7. (withdrawn) The varactor of claim 1 wherein the P- well forms a transistor body, and wherein the transistor body is allowed to float.

8. (withdrawn) The varactor of claim 1 wherein the gate silicon has a width to length ratio of approximately 16 to 1.

9. (withdrawn) The varactor of claim 1 further comprising a first metallization coupled to the gate silicon and a second metallization coupled to the N+ regions.

10. (withdrawn) The varactor of claim 1 wherein the first and second N+/P- junctions extend from a top surface to a bottom surface of the silicon layer.

11. (withdrawn) A varactor comprising:

silicon layer;

a plurality of alternating P- wells and N+ regions in the silicon layer, wherein each P- well forms a first N+/P- junction with the N+ region on one side of the P- well and a second N+/P- junction with the N+ region on the other side of the P- well;

a gate oxide above each of the P- wells; and,

a silicon gate above each of the gate oxides.

12. (withdrawn) The varactor of claim 11 wherein the silicon gate above each of the gate oxides comprises a polysilicon gate above each of the gate oxides.

13. (withdrawn) The varactor of claim 11 wherein the silicon layer is formed over an insulation layer so that the silicon layer and the insulation layer together form an SOI structure.

14. (withdrawn) The varactor of claim 13 wherein the insulation layer is formed over a layer of high resistivity silicon.

15. (withdrawn) The varactor of claim 11 wherein the silicon layer is formed from bulk silicon.

16. (withdrawn) The varactor of claim 11 wherein the silicon layer is formed over a sapphire layer so that the silicon layer and the sapphire layer together form an SOS structure.

17. (withdrawn) The varactor of claim 11 wherein the P- wells form a transistor body, and wherein the transistor body is allowed to float.

18. (withdrawn) The varactor of claim 11 wherein each of the gate silicons has a width to length ratio of approximately 16 to 1.

19. (withdrawn) The varactor of claim 11 further comprising a first metallization coupled to the silicon gate above each of the gate oxides and a second metallization coupled to each of the N+ regions.

20. (withdrawn) The varactor of claim 11 wherein each of the N+/P- junctions extends from a top surface to a bottom surface of the silicon layer.

21-29 (canceled)

30. (withdrawn) A varactor formed by a MOS transistor structure and having a capacitive switching ratio equal to or greater than 5.

31 (canceled)

32. (previously presented) A method of making a varactor comprising:

forming a plurality of alternating P- wells and N+ regions in a silicon layer of an SOI structure, wherein the P- wells form N+/P- junctions with the N+ regions, and wherein each of the P- wells and the N+ regions extends completely through the silicon layer to an insulation layer of the SOI structure;

forming a plurality of gate oxides, wherein each of the gate oxides is formed above a corresponding one of the P- wells;

forming a plurality of silicon gates, wherein each of the silicon gates is formed above a corresponding one of the gate oxides;

electrically coupling each of the silicon gates together; and,

electrically coupling each of the N+ regions together.

33. (previously presented) The method of claim 32 wherein each of the silicon gates comprises a polysilicon gate.

34. (previously presented) The method of claim 32 wherein the SOI structure includes a layer of high resistivity silicon under the insulation layer over.

35. (previously presented) The method of claim 32 where in the insulation layer comprises sapphire.

36. (previously presented) The method of claim 32 where in the insulation layer comprises an oxide.

37. (previously presented) The method of claim 32 wherein the P- wells form a transistor body, and wherein the transistor body is allowed to float.

38. (previously presented) The method of claim 32 wherein each of the silicon gates is formed so as to have a width to length ratio of approximately 16 to 1.

39. (previously presented) The method of claim 32 wherein the varactor has a capacitive switching ratio equal to or greater than 5.

40. (previously presented) The method of claim 32 wherein the varactor has a capacitive switching ratio equal to or greater than 20.